In the claims:

What is claimed is:

1. An input port to a switching core, comprising:

a) an input policing unit that checks if a virtual lane has a sufficient number of credits to carry an input packet received by said input policing unit;

b) a request manager that generates a request for said packet to be switched by a switching core;

c) a packet Rx unit that stores said packet into a memory by writing blocks of data into said memory;

d) a packet Tx unit that receives a grant in response to said request and reads said packet from said memory in response to the grant by reading said blocks of data; and

e) a pointer RAM manager that provides addresses for free blocks of data to said packet Rx unit and receives addresses of freed blocks of data from said packet Tx unit.